We Claim:

1. In a method of designing a circuit containing a plurality of Test Access Port (TAP) interfaces, each said TAP having a Test Data Input (TDI), a Test Data Output (TDO), a Test Mode Select (TMS) input, a Test Clock Input and a Test Reset input (TRSTN), an instruction register and at least one test data register, the method comprising the steps of:

providing a master TAP for at least controlling data transfer operations with other TAPs in said circuit;

connecting master TAP test inputs and output to corresponding circuit test inputs and outputs;

adding to said master TAP:

an instruction register having a length equal to the length of the longest instruction register of each other TAP plus a predetermined number of bits for storing a TAP selection code for selecting one of the TAPs;

a TDO circuit responsive to the TAP selection code for selectively connecting the TDO of one of the TAPs to the circuit TDO; and

for each other TAP:

adding a padding register having a length equal to the length of said master TAP instruction register less the length of the instruction register of said each other TAP and having an input connected to the circuit TDI, and an output;

adding a TMS circuit responsive to a predetermined TAP selection code of said each other TAP for gating TMS pulses applied to the circuit TMS input to said each other TAP;

adding a TDI circuit responsive to a shift state signal for connecting the TAP TDI to either the circuit TDI and or the output of said padding register.

2. A method as defined in claim **1**, further including providing, for said master TAP, an update gating circuit responsive to a predetermined TAP selection code in said selection code register and corresponding to said master TAP for allowing the update of a master TAP update register, and, otherwise, for suppressing the update register except for selection code register bits.

3. A method as defined in claim **1**, further including providing said master TAP with a reset gating circuit for controlling the test reset input of remaining TAPs in said circuit for performing asynchronous and synchronous resets of TAPs, said reset gating circuit effecting an asynchronous reset of said TAPS by transferring an active value of a circuit reset signal applied to said circuit reset input to the reset input of each remaining embedded TAP in said circuit; and effecting a synchronous reset by responding to said master TAP entering a Select-IR-Scan state and application of an active TMS signal to said circuit, by applying an active reset signal to the reset input of each remaining TAP in said circuit.

4. A method as defined in claim **1**, further including, for each test data register shared between two or more TAPs, said test data register having shift register elements responsive to one or more control signals, serial input and a serial output,

adding a first selector having an input for receiving serial input data for each of said two or more TAPS sharing said test data register;

adding a second selector having an input for receiving register control signal bus for each of said two or more TAPS;

each said selector being responsive to said selection code indicative of the source of the serial data and control signal bus to be applied to said shared test dat register, and

connecting said serial output of said shared register to all of said two or more TAPs.

5. A method as defined in claim **1**, further including arranging said TAPS into two or more groups of one or more TAPs, including:

arranging said master TAP in a group in which it is the sole member;

connecting the TDI of said master TAP to the circuit TDI pin;

connecting the output of the TDO circuit to the circuit TDO pin;

providing, in the master TAP, a TDI output for each of the other TAP groups;

connecting the TDO output of each TAP to an input to the TDO circuit; and

providing a padding register for each TAP group whose instruction register chain length is less than the length of the instruction register of the master TAP where the length of the padding register is equal to the length of the master TAP instruction register less the sum of the length of the instruction registers in the group; and

locating each said padding register in an instruction scan path between the circuit TDI and the TAP group TDI.

6. A method as defined in claim **5**, said providing a master TAP including inserting a description of said master TAP into an HDL description file of said circuit.

7. A method as defined in claim **5**, said providing a master TAP including modifying a description of one of said TAPs in an HDL description file of said circuit.

8. A method as defined in claim **5**, said providing a master TAP including selecting an existing TAP in said circuit and modifying said TAP for use as said master TAP.

9. A method of designing a circuit containing a plurality of Test Access Ports (TAPs), each said TAP having a Test Data Input (TDO), a Test Data Output (TDO), a Test Mode Select (TMS) input, a clock input and a Test Reset (TRSTN) input, each said TAP having an instruction register and at least one test data register, the method comprising the steps of:

selecting one TAP as a master TAP;

arranging the remaining secondary TAPs into at least one group having a group TDI and a group TDO, with the TAPs in each group being serially connected in a daisy chain between said group TDI and group TDO;

determining the instruction register length of each said group;

providing said master TAP instruction register with a number of register elements equal to that of the longest group instruction register length plus a number of bits, defining a selection code register, for storing a selection code for use in selecting one of said groups for data transfer;

providing, for each said group, a group padding register having an input connected to the circuit TDI, an output and having a length equal to the length of said master TAP instruction register less the instruction register length of said group;

providing, for each said group, a TMS gating circuit responsive to a circuit TMS input and to a predetermined selection code representative of said group for producing and applying a group TMS signal to each TAP of said group, said group TMS signal being the same as the circuit TMS input when an applied selection code corresponds to the predetermined group selection code corresponding to said group and, otherwise, said TMS signal being inactive, said TMS gating circuit having a TMS input connected to said circuit TMS input; a selection code input connected to said master TAP selection code register and an output connected to the TMS input of all TAPs of the group;

providing, for each said group, a TDI multiplexer circuit for selectively connecting the group TDI to either the circuit TDI when a test data register in the group are being accessed, or to the output of said group padding register when the instruction registers of the group are being accessed and connecting the output of said TDI multiplexer circuit to the group TDI of the first TAP in the daisy-chain;

providing a TDO multiplexer circuit for selectively connecting the group TDO of the group specified by a selection code loaded in said selection code register;

providing, for said master TAP, an update gating circuit responsive to a predetermined group selection code in said selection code register and corresponding to said master TAP for allowing the update of a master TAP update register, and, otherwise, for suppressing the update register except for selection code register bits; and

adding a reset gating circuit to said master TAP for controlling the test reset input of remaining TAPs such that said remaining TAPs are reset when the master TAP is reset.

10. A method as defined in claim **9**, further including adding gating logic for loading a default selection code into said selection code register after a reset.

11. A method as defined in claim **10**, wherein the default selection code is the selection code corresponding to that of the master TAP or any of the groups.

12. A method as defined in claim **9**, said providing a group padding register, including forming said padding register as a portion of the master TAP instruction register.

13. A method as defined in claim **9**, said providing a group padding register including providing a serially connected memory elements between the circuit TDI and the group TDI.

14. A method as defined in claim **9**, wherein the number of groups is two and the number of TAPs in each group is one.

15. A method as defined in claim **9**, further including providing a predetermined number of groups, with each group having one TAP.

16. A method as defined in claim **9**, wherein said TAPs are designed according to the IEEE 1149.1 standard.

17. A method as defined in claim **9**, wherein the resulting circuit is compliant to the IEEE 1149.1 standard.

18. A method as defined in claim **9**, wherein said TDI multiplexer circuit being operable to select between a bypass register and said padding register, said bypass register having of a single memory element connected between the circuit TDI and the TDI multiplexer.

19. A method as defined in claim **9**, wherein the length of said padding register is at least two and its first two shift register elements closest to the circuit TDO capture 0 and 1, respectively, during the execution of a Capture-IR instruction.

20. A method as defined in claim **9**, said TDI multiplexer circuit being operable to select between a bypass register and the output of said padding register, said bypass register having of a single memory element connected between the circuit TDI and the TDI multiplexer; and

the length of said padding register is at least two shift register elements with the first and second shift register elements closest to the circuit TDO capture 0 and 1, respectively, during execution of a Capture-IR instruction.

21. A method as defined in claim **9**, further including, for each test data register shared between two or more TAPs, said test data register having shift register elements responsive to one or more control signals, serial input and a serial output,

adding a first selector having an input for receiving serial input data for each of said two or more TAPS sharing said test data register;

adding a second selector having an input for receiving register control signal bus for each of said two or more TAPS;

each said selector being responsive to said selection code indicative of the source of the serial data and control signal bus to be applied to said shared test dat register, and

connecting said serial output of said shared register to all of said two or more TAPs.

22. In a method of designing a circuit containing a plurality of Test Access Port (TAP) interfaces, each said TAP having a Test Data Input (TDI), a Test Data Output (TDO), a Test Mode Select (TMS) input, a Test Clock Input and a Test Reset input (TRSTN), an instruction register and at least one test data register, the method comprising the steps of:

providing a master TAP for at least controlling data transfer operations with other TAPs in said circuit;

connecting the master TAP test inputs and output to corresponding circuit test inputs and output;

arranging said TAPs into at least two groups of one or more TAPs serially connected between a group TDI and a group TDO, said master TAP being the sole member of one of said groups;

providing said master TAP with:

an instruction register having a length equal to the sum of the length of the instruction registers of the longest group instruction register plus a predetermined number of bits forming a TAP selection code register for storing a group selection code for selecting one of the groups for data transfer;

a TDO circuit responsive to the group selection code for selectively connecting the group TDO of one of the groups to the circuit TDO; and

for each said group:

a padding register having an output connected to the group TDI input of said each group and an input connected to the circuit TDI;

a TMS circuit responsive to predetermined group selection code for said each group for producing a group TMS; and

a TDI circuit responsive to a shift state signal for either connecting a circuit TDI to the group TDI or for connecting the output of said padding register to the group TDI.

23. A method as defined in claim **22**, further including providing, for said master TAP, an update gating circuit responsive to a predetermined TAP selection code in said selection code register and corresponding to the group containing said master TAP for allowing the update of a master TAP update register, and, otherwise, for suppressing the update register except for selection code register bits.

24. A method as defined in claim **22**, further including providing said master TAP with a reset gating circuit for controlling the test reset input of remaining TAPs in said circuit for performing asynchronous and synchronous resets of TAPs, said reset gating circuit effecting an asynchronous reset of said TAPS by transferring an active value of a circuit reset signal applied to said circuit reset input to the reset input of each remaining embedded TAP in said circuit; and effecting a synchronous reset by responding to said master TAP entering a Select-IR-Scan state and application of an active TMS signal to said circuit, by applying an active reset signal to the reset input of each remaining TAP in said circuit.

25. A method as defined in claim **22**, further including, for each test data register shared between two or more TAPs, said test data register having shift register elements responsive to one or more control signals, serial input and a serial output,

adding a first selector having an input for receiving serial input data for each of said two or more TAPS sharing said test data register;

adding a second selector having an input for receiving register control signal bus for each of said two or more TAPS;

each said selector being responsive to said selection code indicative of the source of the serial data and control signal bus to be applied to said shared test dat register, and

connecting said serial output of said shared register to all of said two or more TAPs.

26. A method as defined in claim **22**, said providing a master TAP including inserting a description of said master TAP into an HDL description file of said circuit.

27. A method as defined in claim **22**, said providing a master TAP including modifying a description of one of said TAPs into an HDL description file of said circuit.

28. A method as defined in claim **22**, said providing a master TAP including selecting an existing TAP in said circuit and modifying said TAP for use as said master TAP.

29. In a circuit having a plurality of Test Access Port (TAP) interfaces, each interface having test connections including a Test Data Input (TDI), a Test Data Output (TDO), a Test Mode Select (TMS) input, a Test Clock Input and a Test Reset input (TRSTN), an instruction register and at least one test data register, comprising:

one of said TAPs having test connections serving as a circuit test interface, said one TAP having:

an instruction register having a length equal to the length of the longest instruction register plus a predetermined number of bits for storing a TAP selection code for selecting one of the TAPs;

a TDO circuit responsive to said TAP selection code for selectively connecting the TDO of one of the TAPs to the circuit TDO; and

said one TAP further including, for each other TAP in said circuit:

a padding register having a length equal to the length of said instruction register of said one TAP less the length of the instruction register of said each other TAP and having an input connected to the circuit TDI, and an output;

a TMS circuit responsive to a predetermined TAP selection code associated with said each other TAP and a TMS signal applied to a circuit TMS input for producing a TAP TMS signal for said each other TAP; and

a TDI circuit responsive to a shift state signal for selectively connecting the TDI of said other TAP to the circuit TDI or to the output of said padding register.

30. A circuit as defined in claim **29**, further including a circuit responsive to an active test reset signal applied to said Test Reset input of said one TAP for resetting all of said TAPs

and for performing an asynchronous reset of each said TAP when the finite state machine of said one TAP enters a Select-IR-Scan state and an active TMS signal Is applied to the circuit TMS input.

31. A circuit as defined in claim **29**, further said master TAP further including an update gating circuit responsive to a predetermined group selection code in said selection code register and corresponding to said master TAP for allowing the update of a master TAP update register, and, otherwise, suppressing the update of said update register except for selection code register bits.

32. A circuit as defined in claim **29**, each said TDI circuit for being responsive to an inactive shift state signal of said master TAP for connecting a circuit TDI to the TDI of said each other TAP for accessing a test data register of said each other TAP and responsive to an active shift state signal for connecting said padding register to the TDI of said each TAP for accessing the instruction register of said each TAP.

33. A circuit as defined in claim **32**, said padding register being equal in length to the difference between the length of the instruction register of said one TAP and the length of the instruction register of said each other TAP.

34. A circuit as defined in claim **29**, said TAPs being arranged in at least two groups of serially connected TAPs in which the TDI of each TAP is connected to the TDO of a preceding TAP;

the TDI of the first TAP in a group defining a group TDI and being connected to a respective TAP TDI output of said one TAP; and

the TDO of the last TAP in a group defining a group TDO and being connected to a respective TDO input of said one TAP;

said one TAP being the sole member of one of said groups; said TMS circuit being operable to produce a TAP TMS signal for each TAP of a group.

35. In a circuit having a plurality of Test Access Port (TAP) interfaces, each said TAP having a TAP Test Data Input (TDI), a TAP Test Data Output (TDO), a TAP Test Mode Select (TMS) input, a TAP clock input and a TAP Test Reset (TRSTN) input, a TAP instruction register and at least one TAP test data register, said circuit having a circuit Test Data Input, a circuit Test Data Input, a circuit Test Data Output, a circuit Test Mode Select input, a circuit Test Clock input and a circuit reset input, the improvement comprising:

one of said TAPs being a master TAP;

said TAPs being arranged into at least two groups of one or more TAPs having a group TDI and a group TDO, the TAPs in each said group being daisy-chained between said group TDI and group TDO such that the TDI of each TAP is connected to the TDO of the preceding TAP in the chain, said master TAP being the sole member of one of said groups;

said master TAP having an instruction register bit length equal to the bit length of the longest group instruction register chain length of said groups plus a predetermined number of bits, defining a selection code register, for storing a group selection code for selecting any one of said groups;

a TDO multiplexer circuit responsive to said selection code for selecting the group TDO of the group corresponding to a selection code loaded into said master TAP selection code register for connection to said circuit TDO;

said master TAP having, for each said group:

a padding register having a length equal to the length of said master TAP instruction register less the length of the instruction register chain length of said group, an input connected to the circuit TDI, and an output;

a TDI multiplexer circuit responsive to a shift state signal for selectively connecting said group TDI to either said circuit TDI when a test data register of said group is to be accessed or to said output of said padding register when an instruction register in said group is to be accessed;

a TMS gating circuit responsive to a predetermined group selection code, a predetermined master TAP state signal and said circuit TMS signal for producing and applying a group TMS signal to the TMS input of each TAP in said group, said group TMS signal being the same as the circuit Test Mode Select signal when said current selection code corresponds to said predetermined group selection code or said master TAP is in a reset state, and, otherwise, said group TMS signal being inactive;

an update signal gating circuit responsive to said selection code for suppressing the update of all bits, except for the bits defining said group

selection code, of said master TAP instruction register when the current selection code is other than the predetermined selection code associated with said master TAP and for updating said master TAP instruction register when said the current selection code corresponds to the predetermined group selection code associated with said master TAP;

a reset signal gating circuit responsive to a reset signal applied to the circuit test reset input for controlling the test reset input of said remaining TAPs for resetting said remaining TAPs when said master TAP is reset.

36. A circuit as defined in claim **35**, further including gating logic means for loading a default selection code after a reset.

37. A circuit as defined in claim **36**, wherein the default selection code is the predetermined selection code corresponding to that of the master TAP or any of the groups.

38. A circuit as defined in claim **35**, said padding instruction register for each group including a portion of the instruction register of said master TAP.

39. A circuit as defined in claim **35**, said padding instruction register for each group including memory elements associated with said master TAP and connected in series with the group TDI when an instruction is being loaded into the TAPs of said group.

40. A circuit as defined in claim **35**, wherein the number of groups is two and the number of TAPs in each group is one.

41. A circuit as defined in claim **35**, wherein each said TAPs being compliant with the IEEE 1149.1 Test Access Bus Architecture standard.

42. A circuit as defined in claim **35**, where the resulting circuit is compliant to the IEEE 1149.1 Test Access Bus Architecture standard.

43. A circuit as defined in claim **35**, wherein said TDI multiplexer further selecting between a bypass register and a padding instruction register, the bypass register being comprised of a single memory element connected between the circuit Test Data Input and said TDI multiplexer.

44. A circuit as defined in claim **35**, wherein the length of each said padding register is at least two bits with the first two shift register elements thereof closest to said circuit TDO capture 0 and 1, respectively, during execution of a Capture-IR instruction.

45. A circuit as defined in claim **35**, further including, for each test data register shared between two or more TAPs, said test data register having shift register elements responsive to one or more control signals, and having a serial input and a serial output,

a first selector having an input for receiving serial input data from each of said two or more TAPS sharing said test data register;

a second selector having an input for receiving a register control signal bus from each of said two or more TAPS;

each said selector being responsive to a selection code indicative of the source of the serial data and control signal bus to be applied to said shared test data register,

said serial output of said shared register being connected to all of said two or more TAPs of said circuit.

46. A method of controlling a circuit having a plurality of Test Access Port (TAP) interfaces in which one of said TAPs is connected to circuit test inputs and outputs and each said TAP interface includes a TAP Test Data Input (TDI), a TAP Test Data Output (TDO), a TAP Test Mode Select (TMS) input, a TAP clock input and a TAP reset input (TRSTN), an instruction register and at least one test data register, said TAPs being arranged into two or more groups of TAPs, each group having a group TDI and a group TDO and one or more TAPs serially connected there between, the method comprising:

(a) loading each test instruction into the instruction register of said one of said TAPs, each instruction including a group selection code specifying the TAP to be accessed in the next instruction;

(b) connecting the group TDO of the group having a predetermined TAP selection code corresponding to the TAP selection code stored in said instruction register to the TDO of said circuit;

(c) connecting the group TDI of all groups to the circuit TDI when accessing a test data register of a group;

(d) connecting the group TDI of all groups to a serial output of a respective padding register when an instruction register is to be accessed; and

(e) applying a sufficient number of clock cycles to shift data into said test data register or an instruction into the instruction register of the specified TAP; and

(f) repeating steps (a)-(f) for each additional data transfer operation.

47. A method as defined in claim **46**, wherein step (c) includes connecting the TAP TDI of all TAPs to the circuit TDI in response to an inactive Shift-IR signal during a shift operation.

48. A method as defined in claim **46**, wherein step (c) includes connecting the TAP TDI of all TAPs to the output of a bypass register having an input connected to the circuit TDI in response to an inactive Shift-IR signal during a shift operation.

49. A method as defined in claim **47**, wherein step (d) includes connecting the TAP TDI of all TAPs to a serial output of respective padding registers in response to an active Shift-IR signal during a shift operation.

50. A method as defined in claim **46**, wherein step (e) comprises applying a predetermined number of clock cycles for all instruction loading operations.

51. A program product for use in designing a circuit having a plurality of Test Access Port (TAP) interfaces, each TAP having a Test Data Input (TDI), a Test Data Output (TDO), a Test Mode Select (TMS) input, a Test Clock Input, a Test Reset input (TRSTN), an instruction register and at least one test data register, the program product comprising:

a computer readable storage medium;

means recorded on the medium for reading a circuit description of said circuit having a description of each said TAP;

means recorded on the medium for determining the instruction register bit length of the instruction register of each said TAP;

means recorded on the medium for inserting a description of a master TAP into a description of said circuit including:

connecting master TAP test ports to corresponding circuit test ports;

arranging said TAPs into at least two groups and serially connecting the TAPs in each group between a group TDI and a group TDO with the master TAP being the sole member of one of said groups;

for each group containing secondary TAPs:

connecting the group TDI of each group to a master TAP group TDI output for the group;

connecting the group TDO of each group to a master TAP group TDO input for the group;

determining the instruction register chain length of the group by summing the length of the instruction register bit length of each TAP in the group;

adding to the description of the master TAP:

a master TAP instruction register having a length equal to instruction register chain length of the group having the longest instruction register chain plus a predetermined number of bits forming a TAP selection code register for storing a group selection code for selecting one of the groups for data transfer;

a description of a TDO circuit receiving for input the TDO output of each group and an output connected to the circuit TDO and a select input receiving the group selection code for selectively connecting the group TDO of one of the groups to the circuit TDO; and

for each group:

a description of a padding register having an input connected to a circuit TDI and an output connected to the group TDI of the group;

a description of a TMS circuit responsive to a predetermined group selection code for producing a group TMS; and

a description of said TDI circuit responsive to a shift state signal for either connecting the circuit TDI to the group TDI or for connecting the output of said padding register to the group TDI.